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10/644,215	08/20/2003	Darel N. Emmot	10001763-1	5465
22879 7590 07/15/2009 HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION			EXAMINER	
			NGUYEN, HAU H	
	FORT COLLINS, CO 80527-2400		ART UNIT	PAPER NUMBER
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#### UNITED STATES PATENT AND TRADEMARK OFFICE

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# BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Ex parte DAREL N. EMMOT, BYRON A. ALCORN, and RONALD D. LARSON

Appeal 2008-003212 Application 10/644,215 Technology Center 2600

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Decided: July 13, 2009

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Before KENNETH W. HAIRSTON, ROBERT E. NAPPI, and KARL D. EASTHOM, *Administrative Patent Judges*.

HAIRSTON, Administrative Patent Judge.

#### **DECISION ON APPEAL**

The two month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

Appeal 2008-003212 Application 10/644,215

This is an appeal under 35 U.S.C. §§ 6(b) and 134 from the final rejection of claims 1 to 16. We will reverse.

The disclosed invention relates to a method and system for partitioning state-sequence information, and communicating the partitioned information over a plurality of input/output busses to a computer subsystem. The computer subsystem separately processes the partitioned information received over each of the plurality of input/output busses without first resequencing the information (Figs. 3, 4; Spec. 4 to 7; Abstract).

Claim 1 is representative of the claims on appeal, and it reads as follows:

## 1. A method comprising:

partitioning state-sequenced information for communication to a computer subsystem;

communicating the partitioned information to the subsystem over a plurality of input/output busses; and

separately processing partitioned information received over each of the plurality of input/output busses, without first re-sequencing the information.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Spencer	US 6,311,247 B1	Oct. 30, 2001
Nelson	US 6,801,202 B2	Oct. 5, 2004
		(filed Jun. 28, 2001)
Ebihara	US 6,924,807 B2	Aug. 2, 2005
		(filed Mar. 23, 2001)

The Examiner rejected claims 1 to 15 under 35 U.S.C. § 103(a) based upon the teachings of Nelson and Spencer.

The Examiner rejected claim 16 under 35 U.S.C. § 103(a) based upon the teachings of Nelson, Spencer, and Ebihara.

Nelson transmits sequenced information from host CPU 102 to a computer subsystem (i.e., graphics system 112) via bus 104 (Fig. 2; col. 8, ll. 26 to 28). Unlike the claims on appeal, Nelson partitions the sequenced information after it is communicated to the computer subsystem/graphics system 112 via the single bus (Figs. 3, 21, 22; col. 8, l. 65 to col. 9, l. 24; col. 28, l. 14 to col. 29, l. 12).

The Examiner acknowledges (Ans. 4) that Nelson fails to teach a plurality of I/O busses for communicating the sequenced information to the computer subsystem/graphics system 112. The Examiner contends (Ans. 4), however, that it would have been obvious to one of ordinary skill in the art to use a plurality of input/output busses in lieu of the single bus 104 used by Nelson in view of the plurality of input/output busses (i.e., PCI busses 116 to 118) used by Spencer to interface host 112 to a subsystem. Appellants argue (App. Br. 9, 12) that the skilled artisan would not have made the modification suggested by the Examiner because Spencer is directed to a system that uses each of the PCI busses to interface a single PCI device, and that the information sent by the host to each of the PCI devices via a dedicated PCI bus is for operating each of the PCI devices independently of the other PCI devices. In other words, Spencer is not concerned with partitioning sequenced information and sending such partitioned information to the PCI devices via the PCI busses.

Spencer describes a system in which a plurality of PCI busses 116 to 118 is used to interface a system bus 114 to a plurality of PCI devices (Fig. 2). Each PCI bus is dedicated to transmitting information to only a single

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PCI device (Abstract; col. 3, 1l. 38 to 48; col. 6, 1l. 47 to 49). Spencer is silent as to transmission of partitioned information via the plurality of PCI busses 116 to 118.

Inasmuch as Nelson is silent as to the use of a plurality of I/O busses to communicate partitioned information to a subsystem, and Spencer is not concerned with transmitting partitioned information via the plurality of I/O busses 116 to 118, we agree with Appellants' argument (App. Br. 12) that the applied references neither teach nor would have suggested modifying Nelson to include multiple I/O busses in lieu of the single bus 104. Thus, the obviousness rejection of claims 1 to 15 is reversed because the Examiner's articulated reasons for combining the teachings of the references to Nelson and Spencer do not support a legal conclusion of obviousness. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

The obviousness rejection of claim 16 is reversed because the teachings of Ebihara fail to cure the noted shortcomings in the teachings of Nelson and Spencer.

The decision of the Examiner is reversed.

### <u>REVERSED</u>

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